



THE CRITICAL ROLE OF AN ESD CONTROL PLAN IN PCB ASSEMBLY

Mitigating ESD risk in barcode labeling and masking

Authors:

Tom Rogers, *Technical Director* | Cindy von Recklinghausen, *Senior Product Manager* | Emily Heisig, *Product Manager*



INTRODUCTION

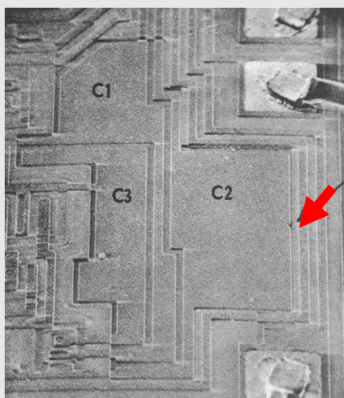
Printed circuit board (PCB) designs are becoming smaller and more complex, with layers of circuitry and components, making the manufacture and assembly of PCBs increasingly challenging. It's imperative that PCBs are designed to meet the intended use and operate flawlessly under adverse conditions and for the life of the device. Meeting these objectives and mitigating risk requires manufacturers to design a device or PCB that can survive and/or tolerate an electrostatic discharge (ESD) event.

The ESD problem in electronics production, and especially PCB assembly, is significant. An ESD event can cause physical damage (e.g., surface oxidation, material loss) to circuits – either printed on the PCB or embedded in a component. ESD can also result in latent defects, resulting in reliability concerns.

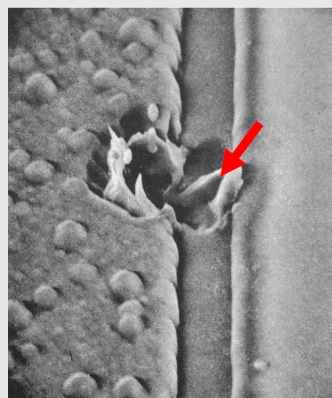
There are many components on PCBs that are vulnerable to ESD, including microcircuits, discrete semiconductors, thick and thin film resistors, and piezoelectric crystals. Precautions are needed in order to prevent damage from an ESD event.^{1,11} ESD damage can be seen immediately during assembly when a circuit stops functioning, or later during the useful life of the device. This latent ESD failure adds to the “cost of ESD” with repair costs, return costs, and end-user disappointment. The industry has estimated that product losses due to ESD can be as high as 7%.³

So, if you didn't think having an ESD control plan was necessary, think again.

FIGURE 1: ESD DAMAGE; C2 MOS MICROCIRCUIT DAMAGE¹³



175X



4300X

UNDERSTANDING STATIC AND ESD SENSITIVITY LEVELS

The main source of static comes when two dissimilar surfaces are brought into contact and then separated. The charge imbalance, or triboelectric charge, on each of the separated surfaces creates an electrical potential that may enable that charge to move. In PCB assembly, there are several key processes that create a triboelectric charge; they include human contact, machine contact (conveyors, robotics, etc.), component mounting, applying solder paste, tape masking and barcode labeling. All sources require consideration when developing your ESD control program.^{2,6,7}

It's important to determine the sensitivity of the PCB and components to electrostatic discharge.

Suppliers (i.e., component manufacturers) provide data for ESD sensitivity levels and characterize

the sensitivity based on exposure to humans and machines using the human body model (HBM) and charged device model (CDM). The main difference between the two models is the rate of discharge, with the human body releasing charges slower than when metal to metal contact occurs in CDM events. Even if humans and machines have the same 5kV potential, the rate of discharge is slower from the human and components may react differently to the discharge rates.^{1,8,11}

As an example, a CMOS component may have an HBM sensitivity of 1000V, but only a 500V CDM. PCB and component manufacturers may use the ESD threshold classification to characterize their part. The following tables (1 and 2) used in the ANSI/ESD/JEDEC JS-002-2014 standard contain the HBM and CDM threshold classifications.^{15, 20}

TABLE 1:
CDM ESDS DEVICE
CLASSIFICATION LEVELS

Classification Level (see note 1)	Classification Test Conditions (in Volts) (see note 2)
C0a	< 125
C0b	125 to < 250
C1	250 to < 500
C2a	500 to < 750
C2b	750 to < 1000
C3	≥ 1000 (See note 3)

Note 1: Use the "C" prefix to indicate a CDM classification level

Note 2: The Classification Test Condition is not equivalent to the actual set voltage of the tester.

Note 3: For Test Conditions above 1,000 volts, depending on geometry of the device package, corona effects may limit the actual pre-discharge voltage and discharge current.

TABLE 2:
HBM ESD COMPONENT
CLASSIFICATION LEVELS

Classification	Voltage Range
0A	< 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

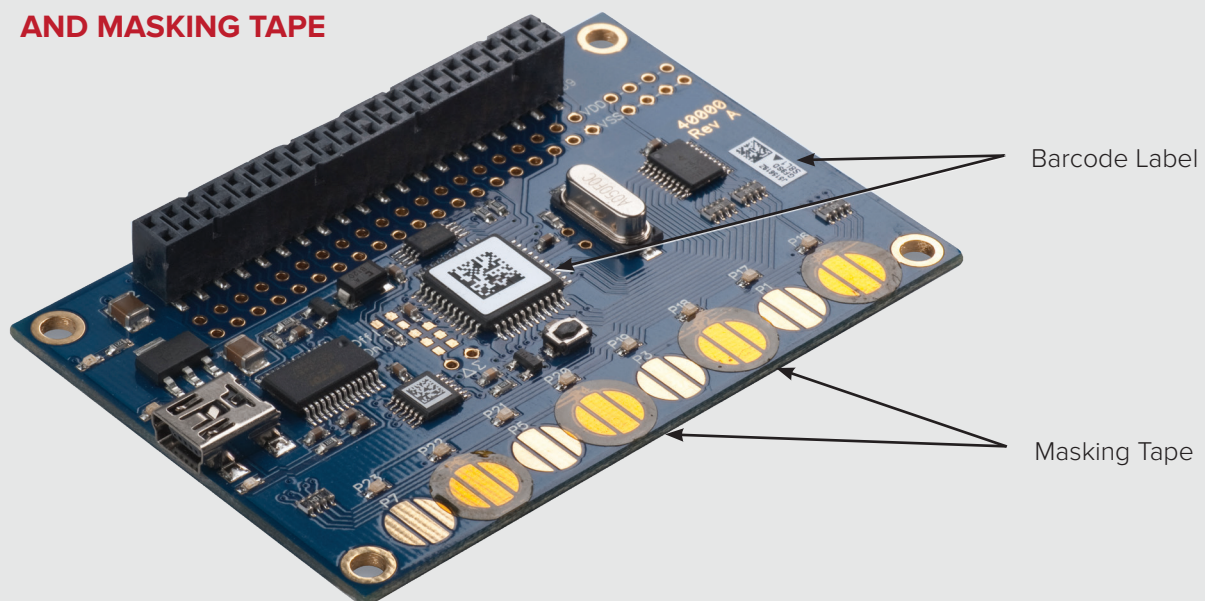
If you are using electronic components that are deemed HBM class 0B or CDM class C0b sensitive, a robust ESD control plan is needed. That plan needs to consider all aspects of PCB assembly and ensure that the following three key elements are defined and resolved: ⁹

1. All conductors need to be grounded. A charged isolated conductor can be a dangerous risk.
2. Non-conductors (insulators) need to be replaced with static dissipative and low charging materials.
3. Transportation of the device outside of ESD protected areas (EPA) requires static protective materials (static safe packaging).

ESD SOURCES: MASKING TAPE AND BARCODE LABELS ^{2,3,4,5,11}

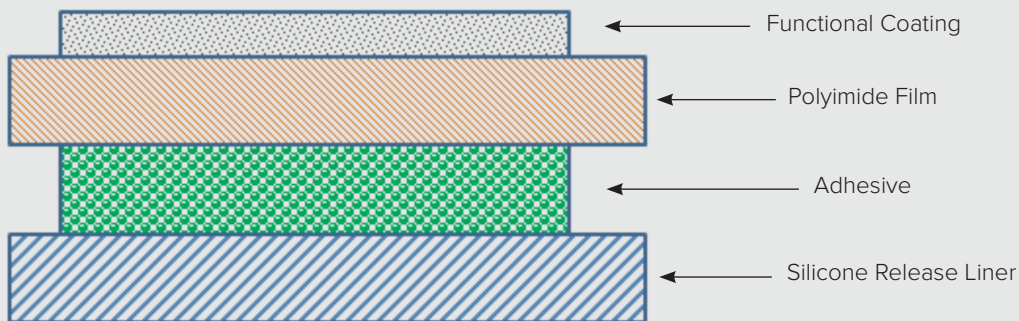
Masking tape and barcode labels play an important role in PCB assembly, but they also create the risk of an ESD event. Masking tape provides protection to components during the assembly process from flux, solder, and cleaning agents. Barcode labels enable tracking of the PCB during the assembly process. Most robust manufacturing processes collect data on the PCB during each assembly step and allow for lot tracking via the barcode. Using a label printed on-demand at the site of manufacture offers a cost effective and flexible way to barcode the PCB.

FIGURE 2:
PCB WITH BARCODE LABEL
AND MASKING TAPE



In PCB assembly, the labels and tapes which are constructed of a film, adhesive, and release liner, are typically cut into small shapes. Since the PCB goes through a harsh set of conditions, including high temperatures and harsh chemical exposures, the tapes and labels use a high temperature film, such as a polyimide or polyester. Typically, the label will have a white coating that allows ink to adhere and provides contrast for scanning the barcode. Similarly, the tape may have a functional coating on the surface of the polyimide film. The following is a typical cross section of a PCB masking tape and barcode label.

FIGURE 3:
BARCODE LABEL AND MASKING TAPE CROSS SECTION.

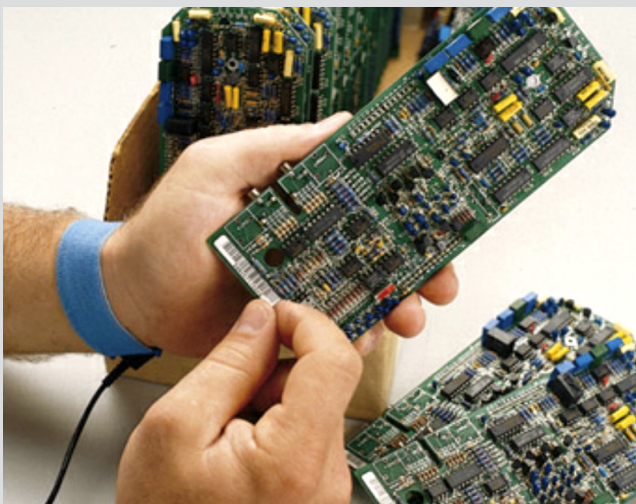


Labels and tapes produce similar static discharge concerns. Before being applied to the PCB, both materials are removed from their release liners. This can be done manually or automatically with a machine. By its nature, the adhesive and liner are poorly bonded, which allows for easy separation. This poor bond is achieved by using a release coating on the liner that is chemically dissimilar to the adhesive. The dissimilar chemistry causes a poor “wetting” of the adhesive that yields the poor bond. However, the dissimilar nature of the adhesive and liner can produce a significant triboelectric charge when separated. During the application process, the charged adhesive will induce a charge in conductive items (including circuitry). Measurements of charge potential of labels and tapes removed from their liners can be greater than 5kV, depending on size.

This charge potential on the adhesive can be amplified by a charge introduced by the human or applicator machine used to apply the material to the PCB. This increases the discharge risk. In addition, the label/ tape being a charged insulator can create a secondary problem. This charge can polarize a neutral PCB or device. This “field induced” charge imbalance on the PCB or device creates a risk of discharge if the PCB is subsequently grounded at an inopportune time.

Another concern with tapes and labels applied to PCBs occurs after application and during the life of the PCB. When the tape or label is applied to the PCB, it can be a source for charge accumulation. As mentioned previously, the tape and label surfaces are either polyimide or have organic coatings that are inherently insulative (i.e., non-conductive). As a result, when the PCB is handled or moved—and the tape or label surface is contacted by a conveyor, human, or robot—there is risk of charge building up on the surface. This charge has the potential for enabling the polarization process described above, which may lead to induction charging and discharging.

FIGURE 4:
APPLICATION OF PCB LABEL BY HAND



Typically, the barcode label is applied for the life of the PCB. However, in some cases, the label is removed. For example, when a PCB is made by a contract manufacturer and the PCB is shipped to another company for final assembly in a device, the label may be removed. In the case of a masking tape, its function is to cover and protect an area on the PCB during assembly. At the end of the process, the tape is removed. The removal of the tape and label provides an ESD concern as charge is created during its removal. The PCB has dissimilar triboelectric charge potentials to the adhesive and a charge can be created on the PCB and the adhesive during removal. This needs to be considered in an ESD control plan.

COMBAT ESD WITH LOW CHARGING AND STATIC DISSIPATIVE TAPES AND LABELS

An ESD control plan should consider “specialized” tapes and labels that have low-charging and static dissipative properties. Both properties will reduce the ESD risk. The following is a description of key tape and label properties and measurements.

1) LOW-CHARGING ADHESIVE SYSTEMS

As mentioned earlier, a key ESD concern is the static charge that is created on the adhesive when it is removed from the liner. The dissimilar nature of the adhesive and liner allows for the adhesive to easily release, but also generates a significant triboelectric charge. To eliminate this charge build-up, there are several techniques that can be employed independently or together:

- **Matching Chemistries:** By using an adhesive and release liner that are chemically similar and also closer on the triboelectric series of materials, you can decrease the charge build-up. While this is theoretically possible, it is difficult to find a system that is chemically similar and will function effectively in the application.
- **Conductive fillers:** By adding conductive fillers to an adhesive, charges will move through a conductive path in the adhesive to a ground. As charges develop when the liner is removed, the charge is removed from the surface of the adhesive. The concern with this technology is that applying a conductive adhesive to the PCB may introduce a short or current leakage to any exposed circuits on the PCB or component.
- **Electric Field Shielding:** When the liner is removed from the adhesive, the resulting charge buildup on the adhesive and liner produces an electric field that surrounds the charge. If shielding is applied in proximity of that separation process, the charge will be reduced. The challenge with this technology is that adding shielding may not be physically possible.

When these types of features are employed in labels and tapes, the resulting reduction in charge build-up on the adhesive can be significant. A common measurement method of this charge build-up is to use a contact voltmeter to measure the voltage level directly on the charged surface. Table 3 shows a comparison of charge build-up in volts for a tape and label with and without the low charging feature. As you can see, the measured voltage of materials with low charging features are significantly lower than those without.

TABLE 3:
PEEL VOLTAGES FOR ADHESIVE ON A TAPE AND LABEL WITH AND WITHOUT LOW-CHARGING FEATURES¹⁴

Tape/Label	Size	Low Charging Feature?	Peel Voltage (Volts)
Polyimide Tape	2"x2"	No	8,000
ESD Polyimide Tape	2"x2"	Yes	< 50
Polyimide Label	2"x2"	No	9,000
ESD Polyimide Label	2"x2"	Yes	< 50

2) STATIC DISSIPATIVE LABEL FACE ^{4,6,7,12}

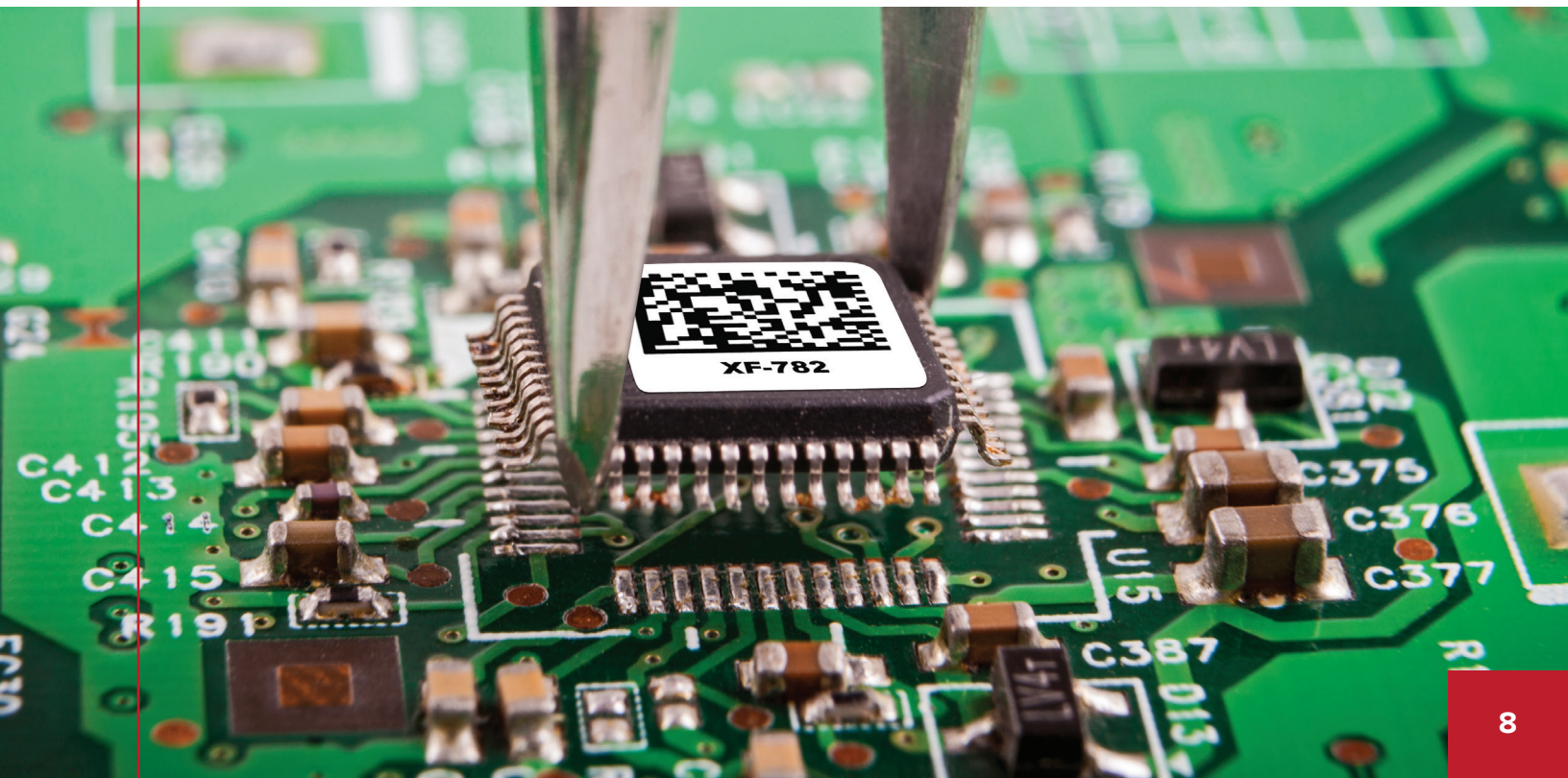
After the label or tape is applied to the surface of a PCB, the insulative face can become a location for charge buildup, especially when handled and/or contacted by conveyors, etc. A way to prevent this charge buildup is to make sure charge movement is allowed over the surface of the tape/label and/or to a ground point. The charge movement should not be fast, but instead gradual to avoid a large electric current being introduced to the PCB.

The standard test method for measuring charge movement or dissipation is ANSI ESD STM11.11. In this method, surfaces are characterized by the speed at which charges move across them: conductive (rapid), dissipative (slow), or insulative (minimal/none).

Table 4 shows the surface resistances that relate to each of the surfaces.

TABLE 4:
SURFACE RESISTANCES FOR MATERIAL TYPES

Surface Type	Charge Movement	Surface Resistance (Ohm)
Conductive	Rapid	$< 10^4$
Dissipative	Gradual	$> 10^4$ to $< 10^{11}$
Insulative	Minimal/None	$> 10^{11}$



The behavior of a charge placed on these surfaces is depicted in Figure 5. If a charge is introduced to a surface by triboelectric charging, it will produce a different level of charge density depending on the surface type.

As seen in Figure 5, if a charge is placed on an insulative surface, it will create an immediate high charge density at the point of contact and that charge will have minimal decay over time. If an equal charge is placed on a conductive surface it will not produce a high charge density because of its rapid dissipation across the surface through electrical conduction. This rapid movement of charge can cause damage to static sensitive devices if the current exceeds design limits. On a dissipative surface, the charge density will be initially lower than on the insulative surface and immediately begins to dissipate slowly across the surface. The dissipation speed helps prevent both high charge densities and rapid discharges, safely neutralizing the charge.

The rate of charge movement is important! A rapid static discharge can be extremely destructive, causing a loss of material or chemical degradation at the point of charge impact as seen in Figure 1. Additionally, a rapid charge movement can cause degradation of a circuit. Gates (switches) used in diodes and transistors can be damaged by exposure to high voltages, reverse voltages, high current or reverse current. This is often called electrical overstress (EOS). Thus, a rapid charge movement (i.e., high current) is to be avoided.

The graph below depicts the rate of charge movement (decay) for each surface type.

FIGURE 5: STATIC CHARGE DENSITY AND DECAY VERSUS SURFACE TYPE

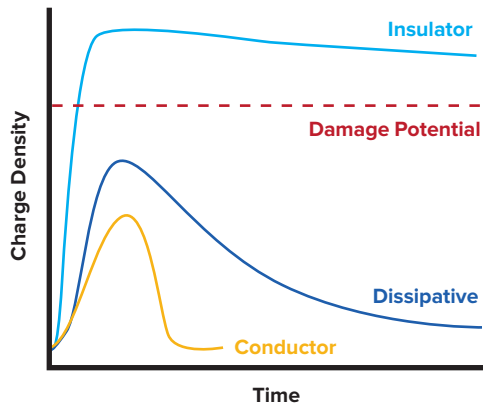
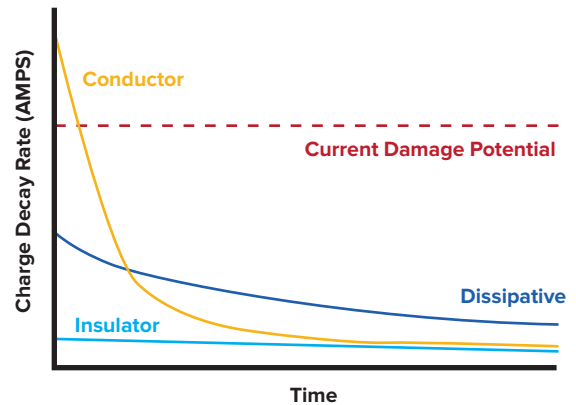


FIGURE 6: CHARGE DECAY RATE VERSUS MATERIAL TYPE



CONCLUSION

Electrostatic discharge (ESD) is a major threat to meeting the short- and long-term performance and reliability requirements of an electronic device. For device manufacturing, and especially during PCB assembly, a robust ESD control plan is an absolute requirement in order to mitigate the risk of ESD failures.

A key element of a successful ESD control plan is to manage the use of charged insulators (e.g., plastics) inside the production environment. Barcode labels and masking tapes are widely used for tracking and protection of electronic devices and are two common charged insulators. The risk of ESD can be reduced by using low-charging and static dissipative label and tape constructions.

POLYONICS ESD-SAFE LABELS AND TAPES

The Polyonics® family of ESD-Safe polyimide and polyester label and tape materials are designed to help protect your most sensitive devices from electrostatic charges arising from both human contact (HBM) and charged devices (CDM). They provide durable static dissipative top surfaces and feature low charging pressure sensitive adhesives (PSA) and liners that generate less than 125 volts with liner removal and again when removed and repositioned.

For more information, please contact us at [603.352.1415](tel:603.352.1415) or info@polyonics.com.

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Polyonics World Headquarters
28 Industrial Park Drive
Westmoreland, NH 03467 U.S.A.

Ph: 603.352.1415
Fax: 603.352.1936
Email: info@polyonics.com

Polyonics Asia
Fuweo Mansion Rm 411
Hongtu Road 88
Nancheng District
Dongguan, Guangdong, China 523078

Ph: 86.755.8825.0441
Fax: 86.755.8825.2429
Email: infoasia@polyonics.com

polyonics.com

